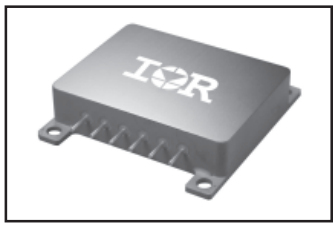
International
IOR Rectifier

PD-97809

D5001R803R3P

26 to 55V Input, Regulated Dual Outputs (+1.8V and +3.3V)

HIGH RELIABILITY, RADIATION TOLERANT, LOW POWER, DC-DC CONVERTER



Description

The D-Series of DC-DC converters are low power radiation hardened, high reliability devices designed for radiation environments such as those encountered by geostationary earth orbit satellites, deep space probes and communication systems. Features include small size, high efficiency, low weight and a high tolerance to total ionizing dose, single event effects, and environmental stresses such as temperature extremes, mechanical shock, and vibration. All components are fully derated to meet the requirements of EEE-INST-002. Extensive documentation including worst case analysis, radiation susceptibility, thermal analysis, stress analysis, and reliability analysis are available.

The D-Series converters have two outputs, each is independently regulated. The outputs can be both positive or one positive and one negative. The D-Series converters incorporate a fixed frequency flyback power stage topology and internal EMI filter. The converters include an enhanced input EMI filter that meets most major satellite power buses. The converters can be remotely turned on and off via an Inhibit pin. Additional Inhibit pins are also provided to control the outputs individually. This feature facilitates turn-on outputs sequencing if desired. Each converter is encased in a cold rolled steel hermetic package. The package measures 1.80"L x 1.40"W x 0.42"H and weighs less than 55 grams.The package utilizes rugged ceramic feed-through copper core pins and is hermetically sealed using parallel seam welding. Two package options are available. Please refer to page 8 for I/O configurations.

Environmental screening includes temperature cycling, constant acceleration, fine and gross leak, and burn-in as specified by MIL-PRF-38534 for class H hybrids.

Non-flight versions of the D-Series converters are available for system development purposes. Variations in electrical specifications and screening to meet custom requirements can be accommodated.

Features

- Total Dose > 50K Rad(Si)
- SEE > 40MeV.cm²/mg
- Low Weight < 55 grams
- 26V to 55V DC Input Range
- Up to 10W Output Power
- Independently Regulated Outputs: +1.8V and +3.3V and Other Outputs Available
- -55°C to +80°C Operating Temperature Range
- 100MΩ @ 100VDC Isolation
- Input Under-Voltage Protection
- Meets Conducted Emission Requirements of Most Major Power Buses:
  100Hz - 100KHz: 80dBμArms
  100KHz - 10MHz: Log-linear Decrease
  10MHz - 50MHz: 40dBμArms
- Short Circuit and Overload Protection
- Meets the Derating Requirments of EEE-INST-002
- Synchronization Input / Output
- On/Off Control via Converters's Inhibit Pin and Individual Output's Inhibit Pin
- High CS Damping

Applications

- Launch Vehicles
- Communication Systems
- Geostationary or Low Earth Orbit Satellites

Circuit Description

The D-Series DC-DC converters utilize two-stage regulation with a flyback topology with a switching frequency of 250KHz for primary regulation and linear post regulation in the secondary for each of the outputs.

Output power is limited under any load fault condition to approximately 110% of rated output. An overload condition causes the converter output to behave like a constant current source with the output voltage dropping below nominal. The converter will resume normal operation when the load current is reduced below the current limit point. This protects the converter from both overload and short circuit conditions. There are no latching elements to eliminate the possibility of falsely triggering the protection circuits during single event radiation exposure.

An under-voltage protection circuit prohibits the converter from operating when the line voltage is too low for safe operation. The converter will not start until the line voltage rises to approximately 20V.

An inhibit pin is provided to control converter operation. This inhibit pin is intended for operation with an open collector transistor drive or a relay closure to the input return. The pin may be left open for normal operation and has a nominal open circuit voltage of 4.0V. Also provided are the individual output on/off control pins (Pin 10, Output 1 Inhibit and Pin 9, Output 2 Inhibit).

Synchronization input pin is included allowing multiple converters to operate at a common switching frequency. Converters can be synchronized to a common frequency with an external clock. This may be used to eliminate beat frequency noise or to avoid generating noise at certain frequencies for noise sensitive systems.

Design Methodology

The D-Series is developed using a proven conservative design methodology, which includes selecting radiation tolerant and established reliability components and fully derating to the requirements of EEE-INST-002. Heavy derating of the radiation-hardened power MOSFET virtually eliminates the possibility of SEGR and SEB.

Specifications

Absolute Maximum Ratings		Recommended Operating Conditions	
Input voltage range	-0.5Vdc to +80Vdc	Input voltage range (Note 13)	26Vdc to 55Vdc
Output power	Internally limited	Output power	0 to Max. Rated
Lead temperature	+300°C for 10sec	Operating temperature	-55°C to +115°C
Operating case temperature (Note 12)	-55°C to +125°C	Operating temperature,	-55°C to +80°C
Storage temperature	-55°C to +135°C	derated (Note 13)	

Electrical Performance Characteristics

Parameter	Group A Subgroup	Conditions -55°C ≤ T_C ≤ +85°C V_{IN} = 42V DC ± 5%, C_L = 0 unless otherwise specified	Limits			Unit
			Min	Nom	Max	
Input Voltage			26	42	55	V
Output voltage (V_{OUT}) (Out 1 / Out 2) 1.8V 3.3V	 1 1	Note 1 I_{OUT} = 100% rated load	 1.782 3.267	 1.800 3.300	 1.818 3.333	 V
1.8V 3.3V	2,3 2,3	I_{OUT} = 100% rated load	1.746 3.200	1.800 3.300	1.854 3.399	V
Output power (P_{OUT}) (Out 1/ Out 2) 1.8V 3.3V	1,2,3	V_{IN} = 26, 42, 55V, Notes 2, 11 Either Output			 2.7 5.0	W
Output power (I_{OUT}) (Out 1/ Out 2) 1.8V 3.3V	1,2,3	V_{IN} = 26, 42, 55V, Notes 2, 11 Either Output	 0 0		 1.5 1.5	A
Line regulation (VR_{LINE}) Each output	1,2,3	V_{IN} = 26, 42, 55V I_{OUT} = 0%, 50%, 100% rated	-0.2		0.2	%
Load regulation (VR_{LOAD}) Each output	1,2,3	I_{OUT} = 0%, 50%, 100% rated V_{IN} = 26, 42, 55V	-0.5		1.5	%
Cross regulation (VR_{CROSS})	1,2,3	V_{IN} = 26, 42, 55V, Note 1			5.0	mV
Input current	1,2,3	I_{OUT} = 0, Pin 6 open Pin 6 connected to Pin 2			35 10	mA
Switching frequency (F_S)	1,2,3		225	250	275	KHz
Synchronization Input Frequency range Pulse high level Pulse low level Pulse transition time Pulse duty cycle	1,2,3	External clock on sync In (Pin 4) Note 1	 450 2.5 -0.5 40 20		 550 5.0 0.5 80	 KHz V V V/µs %

For Notes to Electrical Performance Characteristic Table, refer to page 5

Electrical Performance Characteristics (continued)

Parameter	Group A Subgroup	Conditions -55°C ≤ T_C ≤ +85°C V_{IN} = 42V DC ± 5%, C_L = 0 unless otherwise specified	Limits			Unit
			Min	Nom	Max	
Output ripple (V_{RIP}) Each output 1.8V 3.3V	1,2,3	V_{IN} = 26, 42, 55V I_{OUT} = 100% rated load Note 3			 50 50	mV p-p
Output ripple @ switch frequency	1,2,3	V_{IN} = 26, 42, 55V I_{OUT} = 100% rated load, Note 1		0.5	0.75	mV rms
Efficiency (E_{FF})	1,2,3	I_{OUT} = 100% rated load	45	47		%
Enable Input (Inhibit) Open circuit voltage Drive current (sink) Voltage range	1,2,3	Note 1	 0 -0.5		 4 600 50	 V µA V
Current Limit Point Each output 1.8V 3.3V	1,2,3	V_{OUT} = 90% of Nominal Note 10	 105 105		 145 145	%
Power dissipation load fault (P_D)	1,2,3	Short Circuit, Overload, Note 5			24	W
Output response to step load changes (V_{TLD}) 1.8V 3.3V	4,5,6	Half Load to/ from Full Load, Note 6	 -15 -15		 15 15	mV pk
Recovery time, step load changes (T_{TLD}) 1.8V 3.3V	4,5,6	Half Load to/from Full Load, Notes 6, 7			 500 500	µs
Recovery time, step line changes (T_{TLN})	4,5,6	26V to/from 55V I_{OUT} = 100% rated load, Notes 1, 7, 8			100	µs
Turn-on Response Overshoot (V_{OS}) 1.8V 3.3V Turn-on Delay (T_{DLY})	4,5,6	10% Load, Full Load Note 9	 0.2		 25 25 10	 mV ms
Capacitive Load (C_L) 1.8V 3.3V	1	I_{OUT} = 100% rated load No effect on DC performance, Notes 1, 4 Each output			 220 220	µF

For Notes to Electrical Performance Characteristic Table, refer to page 5

Electrical Performance Characteristics (continued)

Parameter	Group A Subgroup	Conditions -55°C ≤ T_C ≤ +85°C V_{IN} = 42V DC ± 5%, C_L = 0 unless otherwise specified	Limits			Unit
			Min	Nom	Max	
EMC conducted susceptibility (Line rejection)	1	I_{OUT} = 100% rated load Primary power sine wave injection of 2Vp-p, 100Hz to 50MHz, Note 1	80	90		dB
Electromagnetic Interference (EMI), conducted emission (CE)	1	I_{OUT} = 100% rated load, Note 1	Limits per Figure 1			
Isolation	1	Input to Output or Any Pin to Case except pin 3, test @ 50VDC	100			MΩ
Device Weight					55	g
MTBF		MIL-HDBK-217F2, SF, 35°C	1×10^5			hours

Notes: Specification and Electrical Performance Characteristics

1. Parameter is tested as part of design characterization or after design changes. Thereafter, parameter shall be guaranteed to the limits specified.
2. Parameter verified during line and load regulation tests.
3. Guaranteed for a D.C. to 20MHz bandwidth. Tested using a 20KHz to 10MHz bandwidth.
4. Capacitive load may be any value from 0 to the maximum limit without compromising dc performance. A capacitive load in excess of the maximum limit may interfere with the proper operation of the converter's overload protection, causing erratic behavior during turn-on.
5. Overload power dissipation is defined as the device power dissipation with the load set such that both outputs are in a short circuit mode.
6. Load step transition time ≤ 10 µsec.
7. Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within ±1% of its steady state value.
8. Line step transition time ≤100 µsec.
9. Turn-on delay time from either a step application of input power or a logic low to a logic high transition on the inhibit pin (pin 6) to the point where V_{OUT} = 90% of nominal.
10. Current limit point expressed as a percentage of full rated load current.
11. For models with two positive outputs the envelope specification for the design is that each output voltage is limited to the range 1V to 5V.
12. Although operation at temperatures between +85°C and +125°C is guaranteed, no parameter limits are specified.
13. Meets the derating requirements of EEE-INST-002 – except for ceramic capacitors with voltage stress below 10V will minimum be rated at 50V and a minimum load of 20mA on each output.

Device Screening

Test / Inspection	Method	/EM Suffix	Flight (No Suffix)
Element Evaluation	MIL-STD-38534 Class K equivalent with SEM	N/A	X
Nondestructive Bond Pull	MIL-STD-883, Method 2023	N/A	X
Internal Visual	MIL-STD-883, Method 2017	Note 1	X
Temperature Cycling	MIL-STD-883, Method 1010	N/A	Condition C
Constant Acceleration	MIL-STD-883, Method 2001, Y1 Axis	N/A	3000 G's
PIND	MIL-STD-883, Method 2020	N/A	A
Burn-in (2 x 220 hours)	MIL-STD-883, Method 1015	48 Hours @ 115°C	440 Hours @ 115°C
Final Electrical (Group A)	In accordance with device specification	X	X
Seal	MIL-STD-883, Method 1014	Condition A	
Fine Leak			A1
Gross Leak			C
Radiographic	MIL-STD-883, Method 2012	N/A	N/A
External Visual	MIL-STD-883, Method 2009	Note 1	Yes

Notes:
1. Best commercial practice

Radiation Performance Characteristics

Test	Conditions	Min	Unit
Total Ionizing Dose (Gamma) *	MIL-STD-883, Method 1019.5 Operating bias applied during exposure, Full Rated Load, V_{IN} = 50V	50	KRads (Si)
Single Event Effects * SEU, SEL, SEGR, SEB	Heavy Ions (LET) Operating bias applied during exposure, Full Rated Load, V_{IN} = 26, 42, 55V	40	MeV·cm^2/mg

* Test performed at TAMU

International Rectifier currently does not have a DSCC certified Radiation Hardness Assurance Program.

Fig. 1 - EMI Conducted Emission Performance Limit

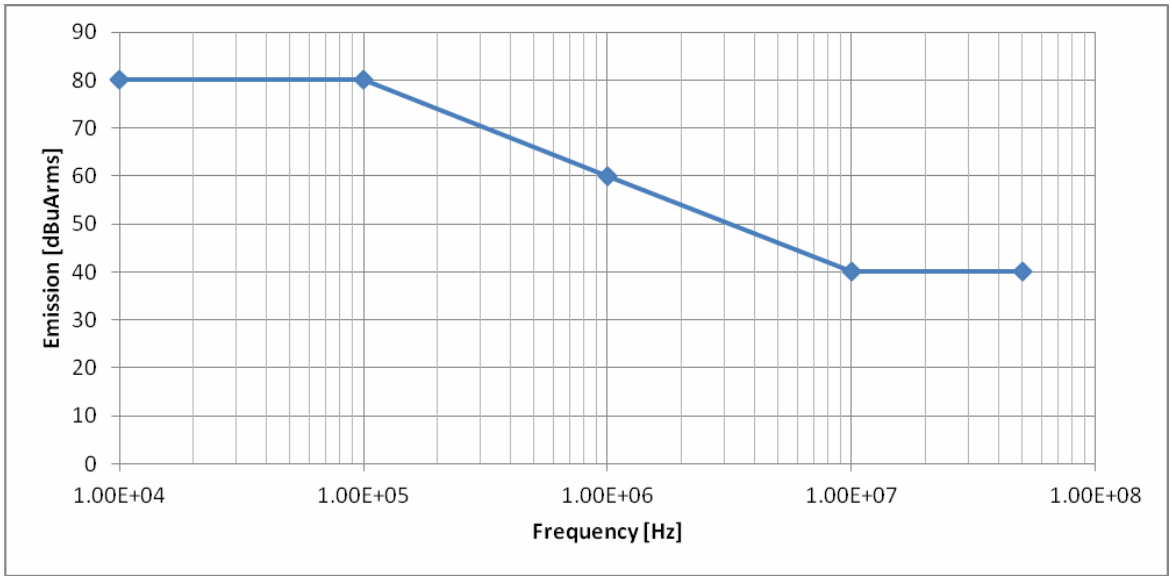
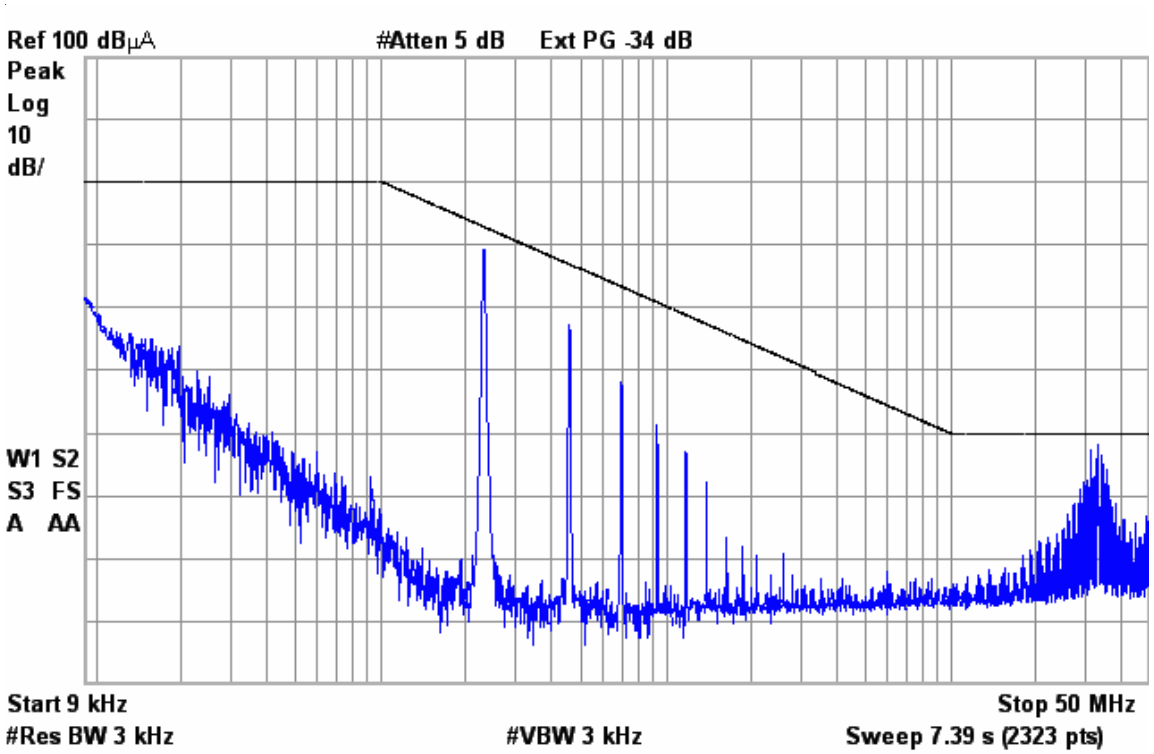
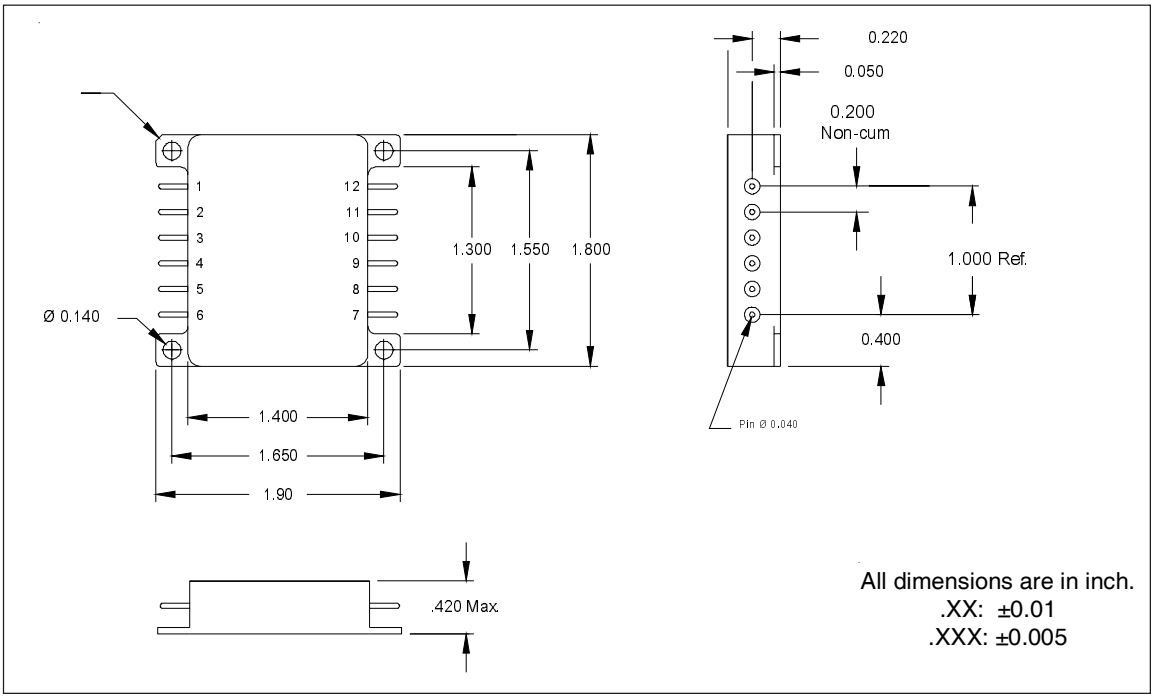


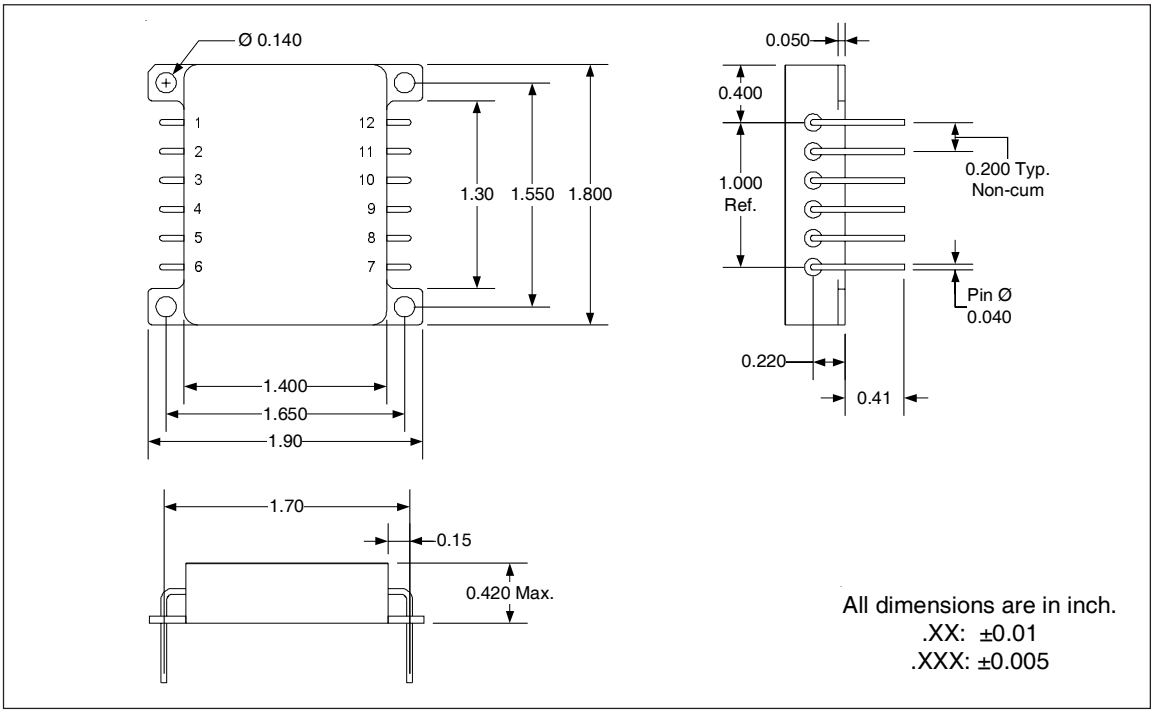
Fig. 2 - A Typical input EMI Conducted Emission Performance



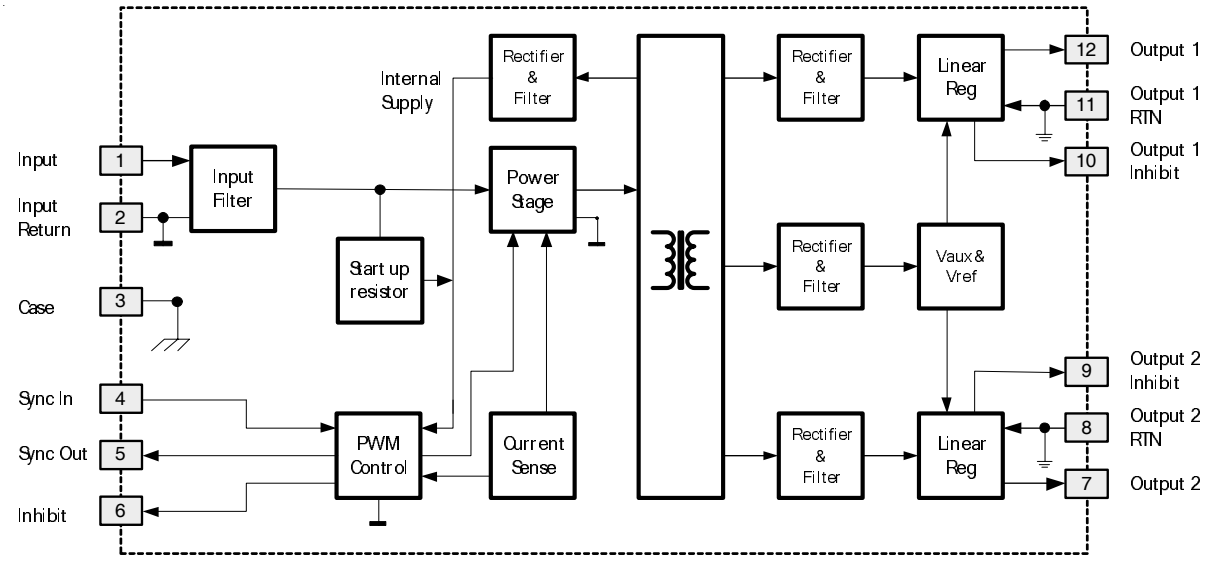
Mechanical Outline - Option A (Straight Pins)



Mechanical Outline - Option B (Down Pins)



Block Diagram

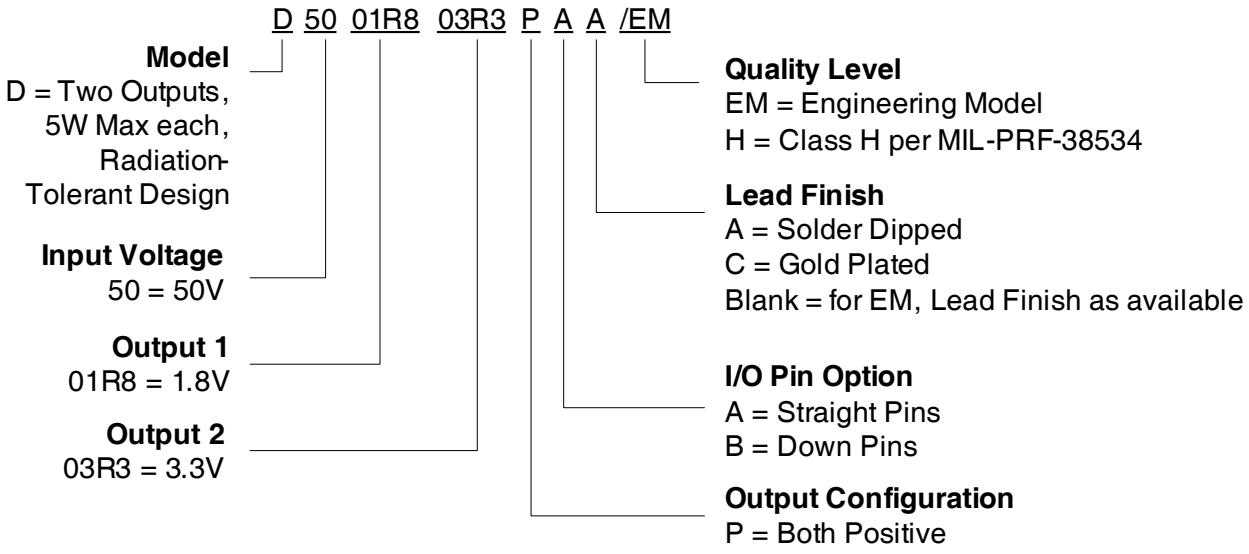


Pin Designation

Pin #	P (Both Outputs Positive)
1	Input
2	Input Return
3	Case
4	Sync In
5	Sync Out
6	Inhibit
7	Output 2
8	Output 2 Return
9	Output 2 Inhibit
10	Output 1 Inhibit
11	Output 1 Return
12	Output 1

Note: Pins 8 and 11 are internally connected

Part Numbering



WORLD HEADQUARTERS: 101 N, Sepulveda Blvd., El Segundo, California 90245, USA Tel: (310) 252-7105
IR SAN JOSE: 2520 Junction Avenue, San Jose, California 95134, USA Tel: (408) 434-5000
Visit us at www.irf.com for sales contact information.
Data and specifications subject to change without notice. 05/2013